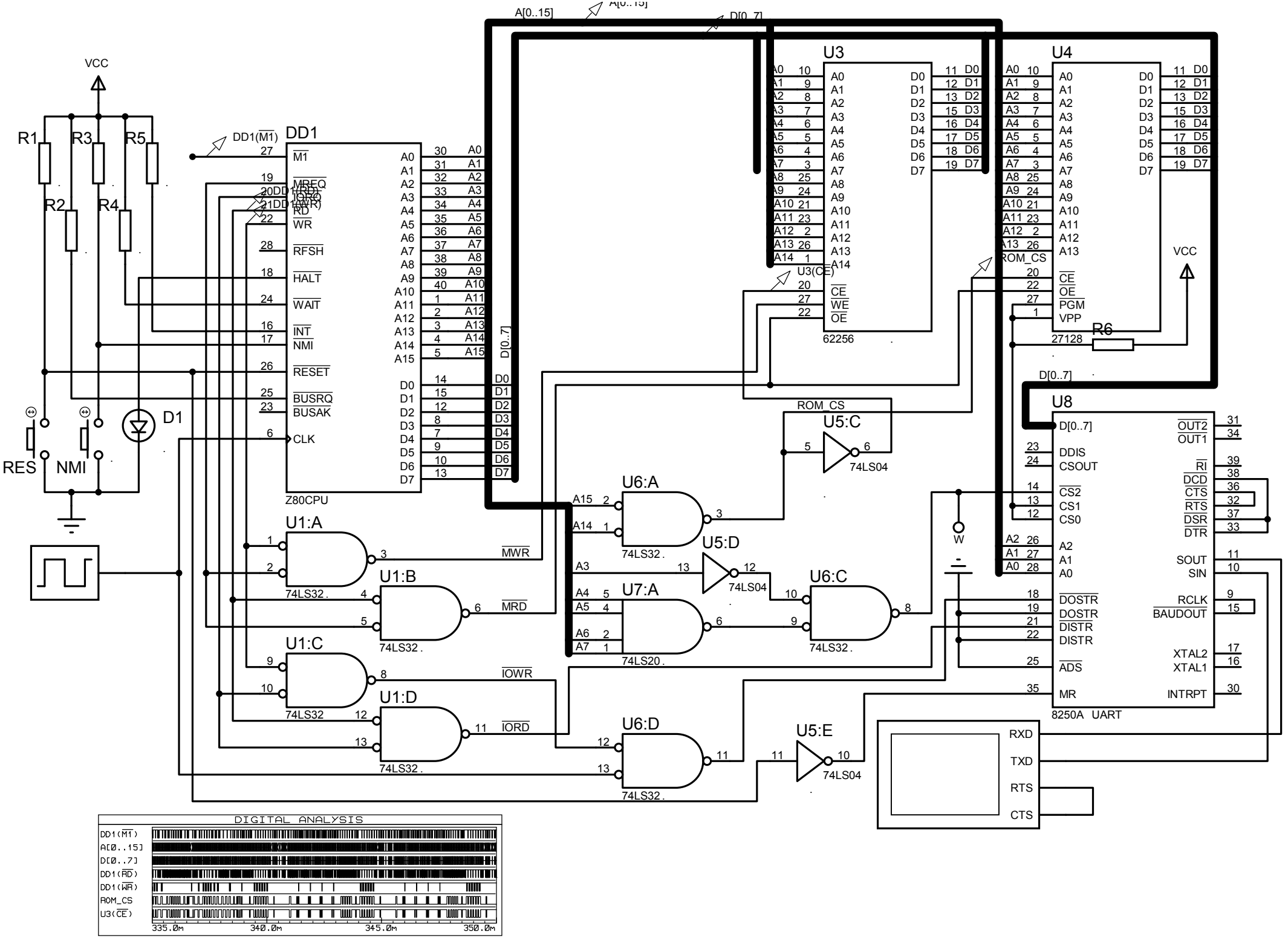
VCC
R1
R3
R5
R2
R4
RES
NMI
D1
DD1
DD1(M1)
M1
MREQ
IORQ
RD
WR
RFSH
HALT
WAIT
INT
NMI
RESET
BUSRQ
BUSAK
CLK
Z80CPU
A[0..15]
D[0..7]
U3
62256
U3(CE)
CE
WE
OE
U4
27128
ROM_CS
R6
U8
8250A UART
D[0..7]
DDIS
CSOUT
CS2
CS1
CS0
A2
A1
A0
DOSTR
DOSTR
DISTR
DISTR
ADS
MR
OUT2
OUT1
RI
DCD
CTS
RTS
DSR
DTR
SOUT
SIN
RCLK
BAUDOUT
XTAL2
XTAL1
INTRPT
W
U1:A
U1:B
U1:C
U1:D
74LS32
MWR
MRD
IOWR
IORD
U6:A
U6:B
U6:C
U6:D
U7:A
74LS32
74LS20
U5:C
U5:D
U5:E
74LS04
ROM_CS
RXD
TXD
RTS
CTS
DIGITAL ANALYSIS
DD1(M1)
A[0..15]
D[0..7]
DD1(RD)
DD1(WR)
ROM_CS
U3(CE)
335.0m
340.0m
345.0m
350.0m